CLAIM AMENDMENTS

1. (Currently Amended) A method for programming an emulator to emulate an integrated circuit (IC) clocked by at least one primary clock signal provided as input to the IC, the IC being described by a netlist as including logic blocks that communicate through synchronizing circuits, wherein the synchronizing circuits include input clock sinks for conveying input signals into logic blocks and output clock sinks for conveying output signals out of logic blocks, and wherein the synchronizing circuits employ clock signals derived from the at least one primary clock signal to clock the input and output clock sinks, the method comprising the steps of:

a. analyzing the netlist to determine a domain, a sub-domain and a phase of each clock signal each synchronizing circuit employs to clock its input and output clock sinks;

b. analyzing the ~~net list~~ netlist to determine a type of each synchronizing circuit based on relationships between the determined domain, sub-domain and phase of the clock signals the synchronizing circuit employs to clock its input and output ~~signals~~ sinks, wherein synchronizing circuit types comprise:

at least one type A synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output clock sinks are derived from at the least one primary clock signal provided as input to the IC and are of similar domain, similar sub-domain and similar phase, and

at least one type B synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output sinks are derived from the at least one primary clock signal provided as input to the IC and are of similar domain, dissimilar subdomain, and similar phase, and

c. modifying the netlist description of each type B synchronizing circuit so that it becomes a type A synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output sinks are derived from the at least one primary clock signal provided as input to the IC and are of similar domain, similar subdomain, and similar phase.

2. (Original) The method in accordance with claim 1

wherein the synchronizing circuits further comprise at least one type C synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output clock sinks are of similar domain, dissimilar sub-domain and dissimilar phase, and

wherein the method further comprises the step of

d. modifying the netlist description of the type C synchronizing circuit so that it becomes a type A synchronizing circuit.

3. (Original) The method in accordance with claim 1

wherein synchronizing circuit types further comprise at least one type C synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output clock sinks are of similar domain, dissimilar sub-domain and dissimilar phase, and

wherein the method further comprises the step of

d. providing an output identifying each type C synchronizing circuit.

4. (Original) The method in accordance with claim 1

wherein the synchronizing circuits further comprise at least one type D synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output clock sinks are of similar domain, similar sub-domain and dissimilar phase, and

wherein the method further comprises the step of

d. analyzing the netlist to determine whether any type D synchronizing circuit has at least one latch as an output clock sink, and

e. providing an output identifying each type D synchronizing circuit having a latch as an output sink.

5. (Original) The method in accordance with claim 1

wherein the synchronizing circuits further comprise at least one type E synchronizing circuit wherein clock signals that clock the

synchronizing circuit's input and output clock sinks are of dissimilar domain, and

wherein the method further comprises the step of:

d. providing an output identifying each type E synchronizing circuit.

6. (Original) The method of claim 1

wherein the synchronizing circuits further comprise at least one type F synchronizing circuit wherein at least one of clock signal clocking any one of the synchronizing circuit's input and output clock sinks resides in more than one clock domain, and

d. providing an output identifying each type F synchronizing circuit.

7. (Original) The method in accordance with claim 1

wherein at least one type B synchronizing circuit comprises:

a least one input sink for clocking at least one input signal into one of said logic blocks in response to a first clock signal;

at least one output sink for clocking at least one output signal out of said one of said logic blocks in response to the second clock signal; and

a clock logic circuit for generating the second clock signal in response to the first clock signal and at least one clock control signal, and

wherein step c comprises modifying the netlist description of the at least one type B synchronizing circuit so that the clock logic circuit generates an enable signal that is a function of the at least one clock control signal, and to convert each of its output clock sinks to an enabled clock sink, wherein each enabled clock sink is clocked by the first clock signal when enabled by the enable signal.

8. (Original) The method in accordance with claim 1

wherein the at least one type B synchronizing circuit comprises:

a least one input sink for clocking at least one input signal into one of said logic blocks in response to a first clock signal;

at least one output sink for clocking at least one output signal out of said one of said logic blocks in response to a second clock signal; and

a clock logic circuit for generating the second clock signal in response to the first clock signal and at least one clock control signal, wherein the clock logic circuit includes at least one flip-flop clocked by the first clock signal, and

wherein step c comprises modifying the netlist description of the at least one type B synchronizing circuit, to convert each flip-flop of the clock logic circuit into a latch, to add a circuit for generating an enable signal in response to a logical combination of the first and second clock signals, and to convert each of the synchronizing circuit's output clock sinks to an enabled output clock sink clocked by the first clock signal only when enabled by the enable signal.

9. (Original) The method in accordance with claim 8 wherein the clock logic circuit is a state machine.

10. (Original) The method in accordance with claim 1 further comprising the step of

d. programming the emulator to emulate an IC described by the netlist as modified at step c.

11. (Original) The method in accordance with claim 2 further comprising the step of

e. programming the emulator to emulate an IC described by the netlist as modified at steps c and d.

12. (Original) The method in accordance with claim 1

wherein the synchronizing circuit types further comprise a type G

synchronizing circuit wherein clock signals that clock the input and output sinks are of similar domain and sub-domain and wherein at least one of the input sinks is clocked on a rising edge and at least one other of the input sinks is clocked on a falling edge, and

wherein the method further comprises the step of

d. providing an output identifying each type G synchronizing circuit.

13. (Original) The method in accordance with claim 12

wherein the synchronizing circuit types further comprise a type H synchronizing circuit wherein clock signals that clock the input and output sinks are of similar domain and dissimilar sub-domain and wherein at least one of the input sinks is clocked on a rising edge and at least one other of the input sinks is clocked on a falling edge, and

wherein the method further comprises the step of

e. modifying the netlist description of each type H synchronizing circuit so that it becomes a type G synchronizing circuit.

14. (Currently Amended) Computer-readable media storing instructions which, when read and executed by a computer causes the computer to carry out a method for programming an emulator to emulate an integrated circuit (IC) clocked by at least one primary clock signal provided as input to the IC, the IC being described by a netlist as including logic blocks that communicate through synchronizing circuits, wherein the synchronizing circuits include input clock sinks for conveying input signals into logic blocks and output clock sinks for conveying output signals out of logic blocks, and wherein the synchronizing circuits employ clock signals derived from the at least one primary clock signal to clock the input and output clock sinks, the method comprising the steps of:

a. analyzing the netlist to determine a domain, a sub-domain and a phase of each clock signal each synchronizing circuit employs to clock its input and output clock sinks;

b. analyzing the ~~net list~~ netlist to determine a type of each synchronizing circuit based on relationships between the determined domain, sub-domain and phase of the clock signals the synchronizing circuit employs to clock its input and output ~~signals~~ sinks, wherein synchronizing circuit types comprise:

at least one type A synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output clock sinks are derived from at the least one primary clock signal provided as input to the IC and are of similar domain, similar sub-domain and similar phase, and

at least one type B synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output sinks are derived from the at least one primary clock signal provided as input to the IC and are of similar domain, dissimilar subdomain, and similar phase, and

c. modifying the netlist description of each type B synchronizing circuit so that it becomes a type A synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output sinks are derived from the at least one primary clock signal provided as input to the IC and are of similar domain, similar subdomain, and similar phase.

15. (Original) The computer-readable media in accordance with claim 14

wherein the synchronizing circuits further comprise at least one type C synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output clock sinks are of similar domain, dissimilar sub-domain and dissimilar phase, and

wherein the method further comprises the step of

d. modifying the netlist description of the C synchronizing circuit so that it becomes a type A synchronizing circuit.

16. (Original) The computer-readable media in accordance with claim 14

wherein synchronizing circuit types further comprise at least one type C synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output clock sinks are of similar domain, dissimilar sub-domain and dissimilar phase, and

wherein the method further comprises the step of

d. providing an output identifying each type C synchronizing circuit.

17. (Original) The computer-readable media in accordance with claim 14

wherein the synchronizing circuits further comprise at least one type D synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output clock sinks are of similar domain, similar sub-domain and dissimilar phase, and

wherein the method further comprises the step of

d. analyzing the netlist to determine whether any type D synchronizing circuit has at least one latch as an output clock sink, and

e. providing an output identifying each type D synchronizing circuit having a latch as an output sink.

18. (Original) The computer-readable media in accordance with claim 14

wherein the synchronizing circuits further comprise at least one type E synchronizing circuit wherein clock signals that clock the synchronizing circuit's input and output clock sinks are of dissimilar domain, and

wherein the method further comprises the step of:

d. providing an output identifying each type E synchronizing circuit.

19. (Original) The computer-readable media of claim 14

wherein the synchronizing circuits further comprise at least one type F synchronizing circuit wherein at least one of clock signal

clocking any one of the synchronizing circuit's input and output clock sinks resides in more than one clock domain, and

wherein the method further comprises:

d. providing an output identifying each type F synchronizing circuit.

20. (Original) The computer-readable media in accordance with claim 14

wherein at least one type B synchronizing circuit comprises:

a least one input sink for clocking at least one input signal into one of said logic blocks in response to a first clock signal;

at least one output sink for clocking at least one output signal out of said one of said logic blocks in response to the second clock signal; and

a clock logic circuit for generating the second clock signal in response to the first clock signal and at least one clock control signal, and

wherein step c comprises modifying the netlist description of the at least one type B synchronizing circuit so that the clock logic circuit generates an enable signal that is a function of the at least one clock control signal, and to convert each of its output clock sinks to an enabled clock sink, wherein each enabled clock sink is clocked by the first clock signal when enabled by the enable signal.

21. (Original) The computer-readable media in accordance with claim 14

wherein the at least one type B synchronizing circuit comprises:

a least one input sink for clocking at least one input signal into one of said logic blocks in response to a first clock signal;

at least one output sink for clocking at least one output signal out of said one of said logic blocks in response to a second clock signal; and

a clock logic circuit for generating the second clock signal in response to the first clock signal and at least one clock control signal, wherein the clock logic circuit includes at least one flip-flop clocked by the first clock signal, and

wherein step c comprises modifying the netlist description of the at least one type B synchronizing circuit, to convert each flip-flop of the clock logic circuit into a latch, to add a circuit for generating an enable signal in response to a logical combination of the first and second clock signals, and to convert each of the synchronizing circuit's output clock sinks to an enabled output clock sink clocked by the first clock signal only when enabled by the enable signal.

22. (Original) The computer-readable media in accordance with claim 21 wherein the clock logic circuit is a state machine.

23. (Original) The computer-readable media in accordance with claim 14 wherein the method further comprises the step of

d. programming the emulator to emulate an IC described by the netlist as modified at step c.

24. (Original) The computer-readable media in accordance with claim 23 wherein the method further comprises the step of

e. programming the emulator to emulate an IC described by the netlist as modified at steps c and d.

25. (Original) The computer-readable media in accordance with claim 14

wherein the synchronizing circuit types further comprise a type G synchronizing circuit wherein clock signals that clock the input and output sinks are of similar domain and sub-domain and wherein at least one of the input sinks is clocked on a rising edge and at least one other of the input sinks is clocked on a falling edge, and

wherein the method further comprises the step of

d. providing an output identifying each type G synchronizing circuit.

26. (Original) The computer-readable media in accordance with claim 25

wherein the synchronizing circuit types further comprise a type H synchronizing circuit wherein clock signals that clock the input and output sinks are of similar domain and dissimilar sub-domain and wherein at least one of the input sinks is clocked on a rising edge and at least one other of the input sinks is clocked on a falling edge, and

wherein the method further comprises the step of

e. modifying the netlist description of each type H synchronizing circuit so that it becomes a type G synchronizing circuit.

27-29 (Canceled)